FORM PTO-1449	SERIAL NO.	CASE NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	To be Assigned	9281-4682
(use several sheets if necessary)	FILING DATE: Herewith	GROUP ART UNIT
	APPLICANT(S): Hiroyuki Sakamoto et al.	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES	TRANSLATION NO
	A1	08-236652	09/1996	JAPAN		X	
	A2	08-213498	08/1996	JAPAN		X	
	A3	11-233537	08/1999	JAPAN		X	
	A4	2506028	05/1996	JAPAN		X	

EXAMINER INITIAL		OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Rev. Oct. 97

"Express Mail" mailing label number EV 327 137 080 US
Date of Deposit 10/21/03

Our File No. 9281-4682
Client Reference No. S US02272

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hiroyuki Sakamoto et al.

Serial No. To Be Assigned

Filing Date: Herewith

For: Circuit Device Resistant to Cracking And Having Sealing Layer Resistant to Sagging And Method for Making The Same

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the obligation under 37 C.F.R. 1.56 and in conformance with 37 C.F.R. 1.97-1.99, Applicants hereby submit references A1-A4 listed on the attached form PTO-1449 for consideration by the Examiner. Copies of the references are enclosed herewith.

Japanese Unexamined Published Patent Application No. H08-236652 discloses a construction of a circuit part in which a semiconductor chip is mounted on a substrate and a shield member for shielding the semiconductor chip is attached.

Japanese Utility Model No. 2506028, Japanese Unexamined Published Patent Application No. H08-213498 and H11-233537 disclose a construction of a circuit part in which a semiconductor ship is mounted on a substrate and the semiconductor chip is sealed.

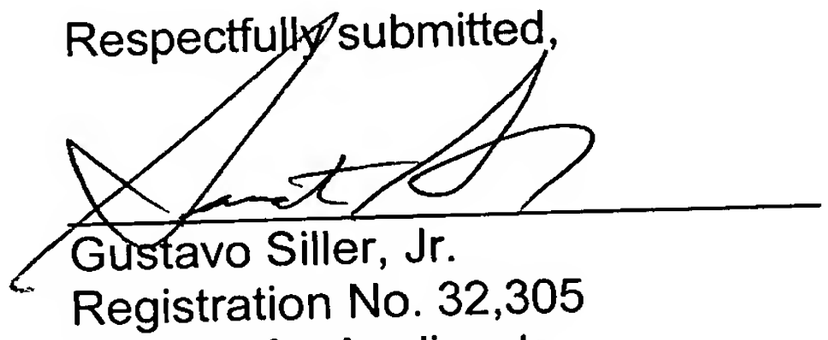
The filing of this Information Disclosure Statement does not constitute an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. Section 1.56(b). Further, Applicants reserve the

right to contest these references as prior art against the present application, and Applicants do not believe that the disclosure of these references, even if finally determined to be prior art, anticipates Applicants' invention or that these references make Applicants' invention obvious.

No fees are believed to be due in connection with filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this material, the Commissioner is hereby authorized to deduct said fees from Brinks Hofer Gilson & Lione Deposit Account No. 23-1925.

Applicants respectfully request that the Examiner review the entire disclosure of these documents and make them of record.

Respectfully submitted,



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